21. (Unchanged) A data collector circuit consisting of an intrinsically safe circuit according to claim 1 or claim 12.

REMARKS

Twenty-one claims were originally filed in this case, and all claims were rejected. Claim 8 has been canceled. Claims 1, 3-7, 10-12, and 14-17 have been amended. Reconsideration of the application in view of the above changes and the following remarks is respectfully requested.

On page 2 of the Office Action, the Examiner noted the proper language and format for the abstract of the disclosure and that it should not include legalese and repeat information. Applicants have amended the abstract to remove legalese and repeat information. Applicant submits that no new matter has been added by the above changes to the abstract.

On page 2 of the Office Action, the Examiner rejected claims 1-21 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter applicant regards as the invention. In particular, the Examiner noted terms that lack antecedent basis, grammatical errors and indefinite terms in claims 1, 3-7 12, 14 and 15. Applicant has corrected all these noted defects with the above amendments to claims 1, 3-7, 10-12, and 14-17. Applicant submits that claims 1-21 now describe the invention with sufficient particularity to be patentable, and request that the rejection under § 112, second paragraph be withdrawn.

On page 3 of the Office Action, the Examiner rejected claims 1-7 and 9-21 under 35 U.S.C. § 102 as being anticipated by Hoeflich et al., U.S. Patent No. 4,954,923. The Examiner also rejected claim 8 under 35 U.S.C. § 102 as being obvious over Hoeflich et al. Claim 8 has been canceled. The Examiner contends that Hoeflich et al. teaches a plurality of sectors 34, 38, 20 , a power limiting means MPA (resistor 25) , and a voltage clamping means 27-29.

Applicant has amended claims 1, 10, 16 and 17 similarly and now each specifies that the plurality of circuit sectors are located in the hazardous environment. Claim 1 recites:

> An intrinsically safe circuit for use in a hazardous environment, the circuit comprising: a **plurality of circuit sectors for location in the hazardous environment** and which are substantially isolated physically from one another by electrical insulating means, and are **electrically connected, directly or indirectly, so as to define at least one power transfer path between each said circuit sector and at least one other said circuit sector, and power limiting means provided in each said power transfer path between at least two said connected circuit sectors** for limiting a maximum power transfer value therebetween to a value less than a predetermined threshold value at which combination in said hazardous environment is initiated. (emphasis added).

The claimed invention is particularly advantageous because the claimed circuit **allows power transfer** to take place between circuit elements or modules **in the hazardous area** by designing the circuit in separate circuit sectors and providing power limiting means between at least two circuit sectors which have power transfer path(s) therebetween, in order to limit the maximum power transfer value therebetween to a value less than the predetermined threshold value at which combustion in the hazardous environment is initiated. There is no such teaching in Hoeflich et al.

The claims are patentably distinct over Hoeflich et al. since there is no teaching in Hoeflich or any suggestion therein that the "circuit sectors" (namely display module 17, and CMOS logic modules 34) can communicate with each other at all, other than via the datacom paths in the safe area. Since none of the circuit sectors in Hoeflich are allowed to communicate with one another (and therefore potentially allow power transfer therebetween) in the hazardous area, there is no need for Hoeflich to consider the problems associated with potential power transfer between the sectors in the hazardous area.

Another significant point about Hoeflich is that communication between circuit elements in the master module 15 (in the hazardous area) and the datacoms and associated current loops with barriers 12 (in the safe area) is only possible via opto-couplers 53. Opto-couplers **do not allow power transfer** and thus in fact the opto-couplers 53 effectively prevent any power transfer taking place between the CMOS logic modules 34, via the data communication paths and associated current loops in the safe area.

Thus, Hoeflich in fact teaches entirely away from the present invention by specifically preventing the possibility of any potential power transfer taking place between the modules 34, via the datacomms paths. In contrast, the present invention envisages a circuit in which power transfer can take place between various circuit sectors, but power-limiting means (e.g. resistor) are provided in the power transfer path(s) to limit the maximum power transfer which can take place between sectors, to an acceptable level.

Applicant also disagrees with the Examiners characterization of Hoeflich et al. First, the power supply 10 of Hoeflich et al. is not a "circuit sector" since as now claimed the

"circuit sectors" must be located in the hazardous environment. Second, the MPAs 21, 24 used in the Hoeflich circuit **cannot** be considered as power limiting means provided in a power transfer path between at least two circuit sectors for location in the hazardous area, as required by the amended claim 1 because they do not connect two "circuit sectors" in the hazardous area. Third, the DSAs 38 in Hoeflich do not constitute power limiting means in power transfer paths between the CMOS modules 34 and the loads 17. Each DSA 38 is a resistor in series with the data comms circuits and current loops in the safe area, to provide attenuation for the data communications wiring (see column 3, lines 35-38, and column 6, lines 51-64). There is no power transfer path between the CMOS modules 34 and the loads 17. For these additional reasons, Applicant submits that claims are not anticipated or made obvious by Hoeflich et al.

With reference to Hoeflich, applicants submit that, significantly, the only power transfer paths in the Heoflich circuit (see Fig. 1) are: (a) between the power supply 10 and the load modules 17; (b) between the power supply 10 and CMOS logic modules 34 in the master module 15; and (c) from the data communications paths and current loops associated with the barrier devices 12, to the load modules 17 (via the master module 15). Both the power supply 10 and the datacomms paths and associated current loops are located in a **dedicated safe area** (see Fig. 1 of Hoeflich).

There are no power of transfer paths **in the hazardous area** between any of the display modules 17, or between any of the CMOS logic modules 34 and the display modules 17 (there are only data communication paths between CMOS logic modules 34 and display modules 17). Moreover, there is no power transfer path between any of the load modules 17

connected to the ISMI slave mdoule 20, and any of the other loads 17 or CMOS modules 34. There is only a power transfer path between the load modules 17 and the power supply 10 (or datacomms paths and current loops associated with barriers 12).

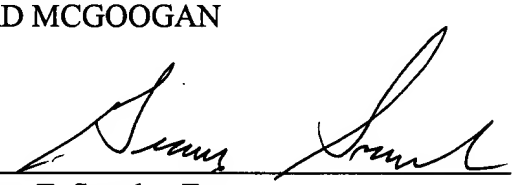
Applicants notes that power limiting means in the form of an MPA 21 is supplied in each power transfer path between a display module 17 and the power supply 10 (see column 6, paras, 3-4). An MPA 24 is also supplied in the power transfer path between the power supply 10 and the CMOS logic modules 34. Power limiting means in the form of an opto-coupler 53 is also provided in each power transfer path between a CMOS logic module 34 and the data communications paths and associated current loops and barriers 12. Significantly though, the power supply 10 and the data communications paths are both located **outside the hazardous area**, in a dedicated safe area (see column 4, lines 56-60). So no power transfer takes place at all between any of the loads or circuit modules actually located in the hazardous area. This is in direct contrast to the present invention in which at least one power transfer path exists between each claimed circuit sector and at least one other circuit sector, all the circuit sectors being located in the hazardous area.

Claims 2-7, 9, 11-15, and 18-21depend, either directly or indirectly from claims 1, 10, 16 and 17, respectively. Claims 2-7, 9, 11-15, and 18-21 also include recitations that further defined the claimed invention. Based on their dependence on claims 1, 10, 16 and 17 and other patentable recitations, claims 2-7, 9, 11-15, and 18-21 are also believed to be patentable.

Applicant respectfully requests a two-month extension of time in responding to the above-identified office action and has also enclosed a check for the requisite fee for the two-month extension of time in responding to the above-identified office action.

In view of the foregoing arguments, Applicants respectfully submit that the claims presently in this case are now in condition for allowance. Reconsideration and prompt favorable action are therefore solicited.

Respectfully submitted,
GERARD MCGOOGAN

By: 

Greg T. Sueoka, Esq.
Registration No. 33,800
Fenwick & West LLP
Two Palo Alto Square
Palo Alto, CA 94306
(650) 858-7194 (Phone)
(650) 494-1417 (Fax)

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